## Application/Control IV. Applicant(s)/Patent Under Reexamination GRANSTON ET AL. Examiner Art Unit Page 1 of 1

## **U.S. PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	Α	US-6,240,509	05-2001	Akkary, Haitham	712/228
	В	US-5,930,492	07-1999	Lynch, Thomas W.	712/216
	C	US-			
	D	US-			
	Е	US-			
	F	US-			
	G	US-			
	Н	US-			
	-	US-			
	J	US-			
	К	US-			
	L	US-			
	М	US-			

## FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	0					
	Р					
	Q					
	R					
	s					
	Т					

## NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)				
	U	Schlansker et al., "Achieving High Levels of Instructions-Level Parallelism with Reduced Hardware Complexity", Nov 1994, HPL-96-120, www.hpl.hp.com/techreports/96/HPL-96-120.pdf				
	٧	Rau et al., "Code Generation Schema for Modulo Scheduled Loops", ACM Proceedings of the 25th annual International Symposium on Microarchitecture, Dec 1992, volume 23, iss. 1-2				
	w	Rau et al., "Register Allocation for Software Pipelined Loops", June 1992, In Proc. of the ACM SIGPLAN'92 Conference on Programming Language Design and Implementation, pages 283-299				
	х					

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)

Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.